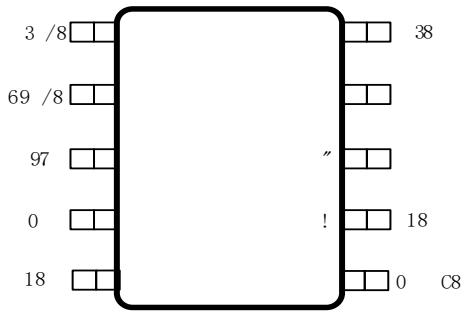
Figure 9 and 10.

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DISCRIPTION	MSL
SCT81621MRDR	Tape & Reel	4000	1621	10	10-Lead 3mm×3mm Plastic MSOP	3

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, UVLO_EN	-0.3	62	V
VCC, DR (DC voltage)	-0.3	6.6	V
VCC, DR (Transient for <20ns)	-1	7.0	V
ISEN, COMP, FB, FA/SYNC/SD	-0.3	5.5	V
Peak Driver Output Current		1	



Top View: 10-Lead Plastic MSOP 3mmx3mm

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NAME	NO.	DESCRIPTION
FA/SYNC/SD	6	Switching frequency setting pin. The switching frequency is programmed by a single resistor between this pin and AGND. The internal clock can be synchronized to an external clock. A high level on this will then draw 3.9 µA from the supply typically.
PGND	7	Power ground pin.
DR	8	N-channel MOSFET gate drive output. Connect directly to the gate of the N-channel MOSFET through a short, low inductance path.
VCC	9	Output of the internal VCC regulator and supply voltage input of the MOSFET driver. Connect a ceramic bypass capacitor from this pin to PGND.
VIN	10	Power supply input pin Connect a ceramic bypass capacitor from this pin to PGND.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.1	50	V
V_{CC}	VCC voltage range	3.1	6.1	V
T_J	Operating junction temperature	-40	125	°C

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V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.1		50	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		2.8	–	V
	Hysteresis			160		mV
I_{SD}	Shutdown current	$V_{FA/SYCN/SD}$=5V or V_{UVLO_EN}=0		3.9	8	uA

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V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
C_{HICCUP}	Hiccup mode off-time after activation	Clock cycles with no				

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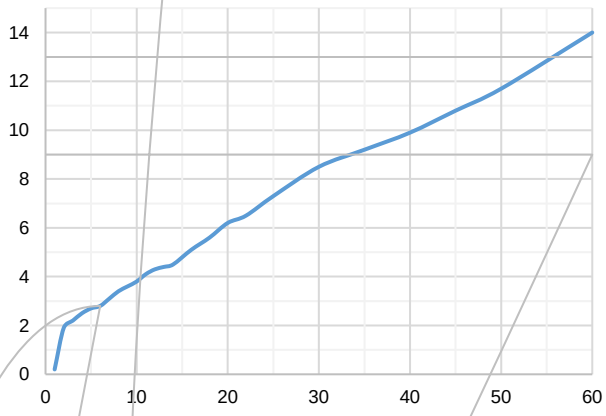


Figure 1. I_{SD} vs. Input Voltage

Figure 2. I_Q vs. Input Voltage

Figure 3. Switching Frequency vs. RT

Figure 4. Switching Frequency vs. Temperature

Figure 5. Efficiency vs. Load Current, Boost, V_{OUT}=12V

Figure 6. Efficiency vs. Load Current, SEPIC, V_{OUT}=12V

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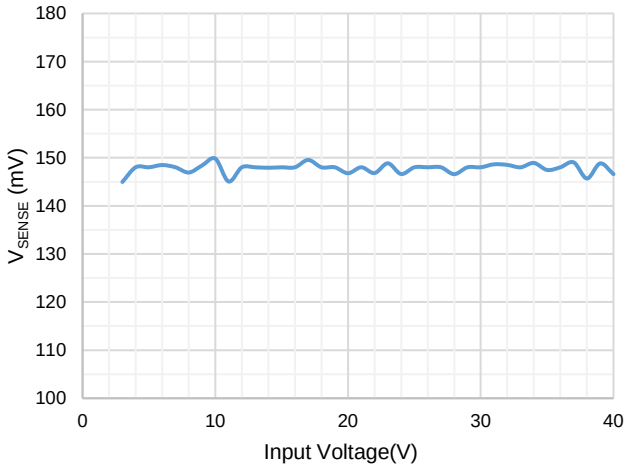


Figure 7. Current Sense Threshold vs. Input Voltage

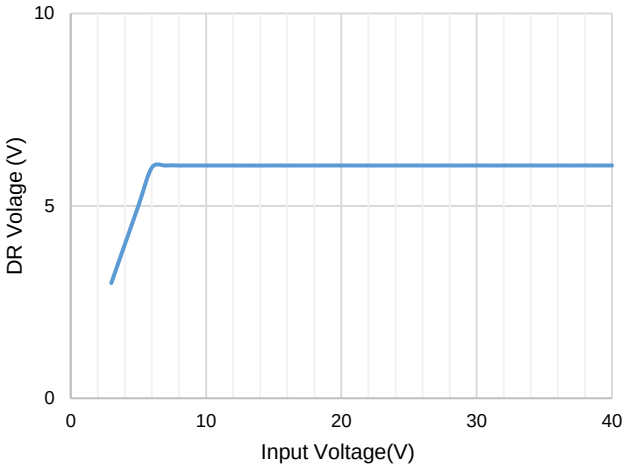


Figure 8. DR Volage vs. Input Voltage

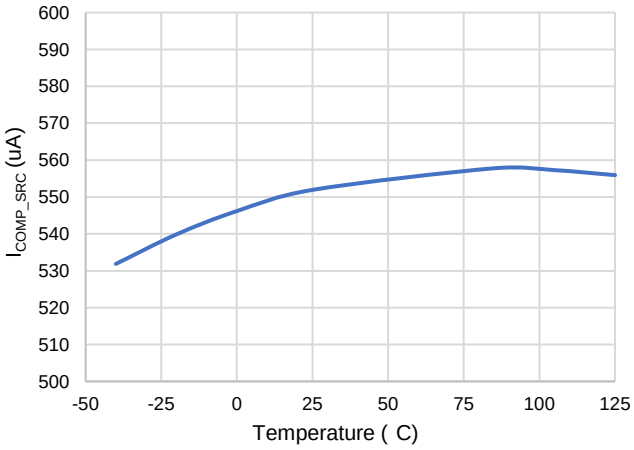


Figure 9. COMP Source Current vs. Temperature

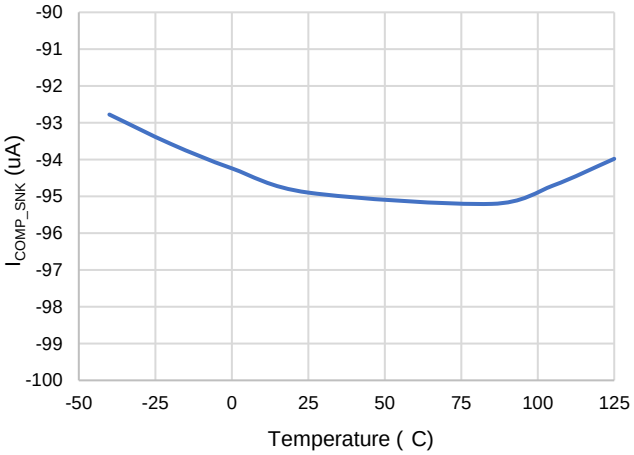


Figure 10. COMP Sink Current vs. Temperature

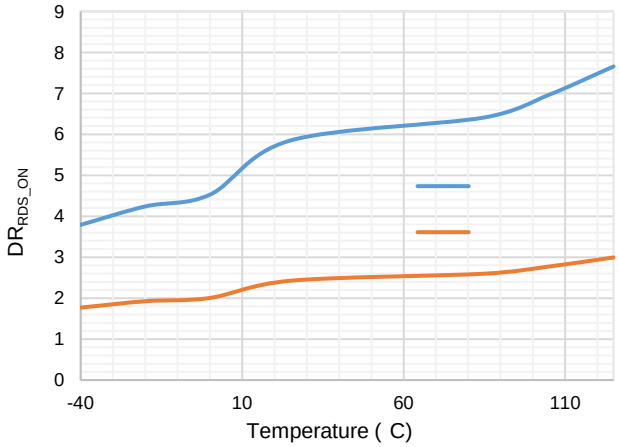


Figure 11. DR Resistance vs. Temperature

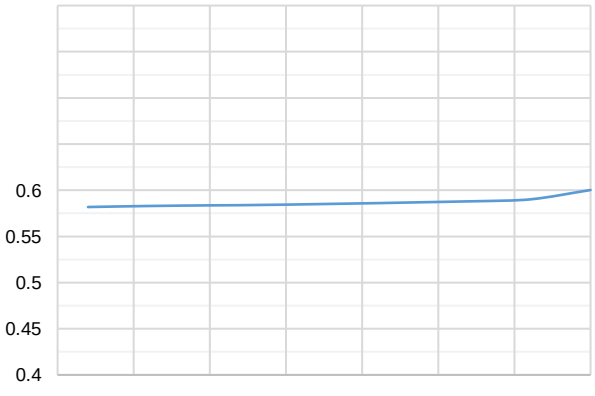


Figure 12. Shutdown Threshold Hysteresis vs. Temperature

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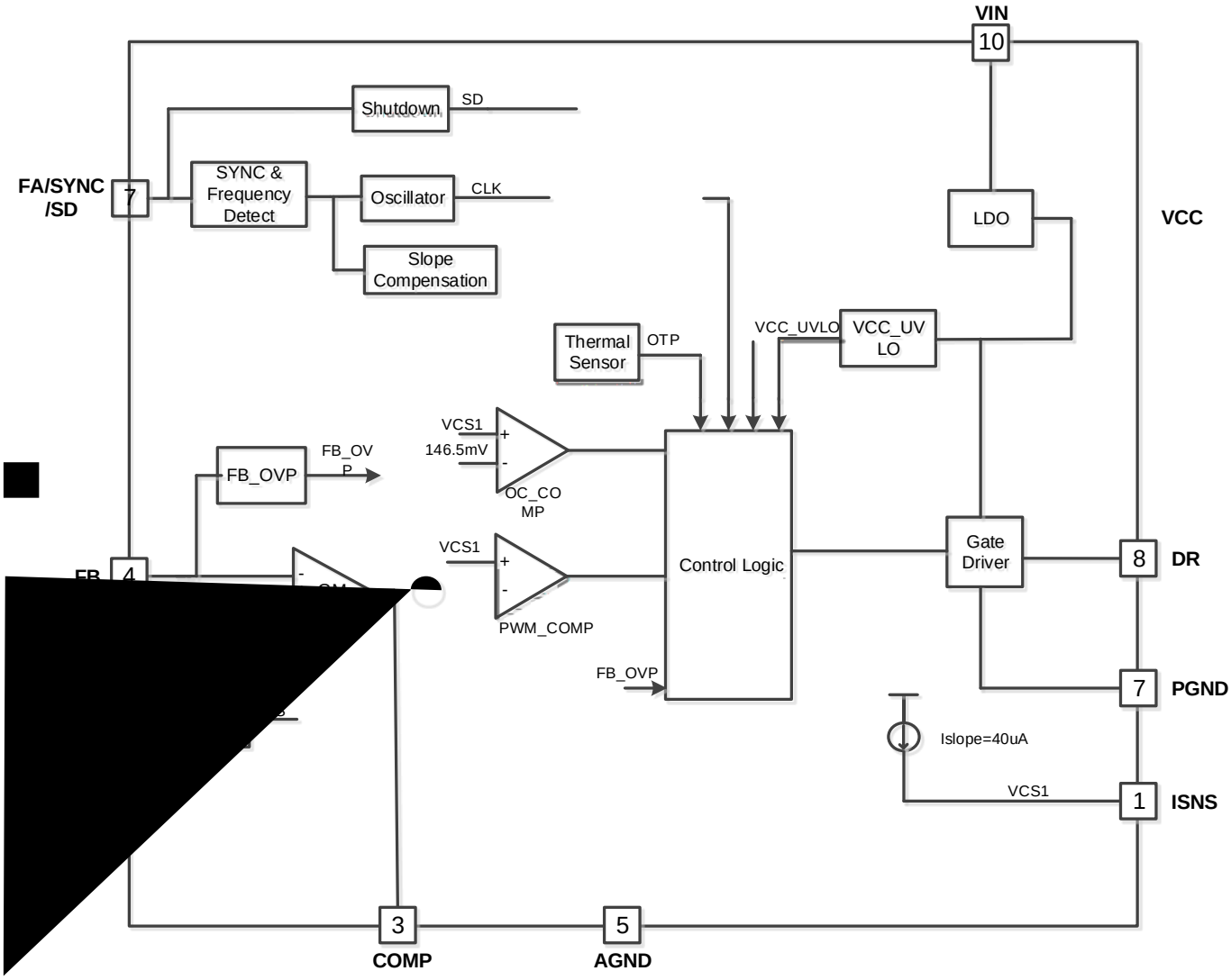

VIN
10
Shutdown
SD
FA/SYNC
/SD
7
SYNC &
Frequency
Detect
Oscillator
CLK
Slope
Compensation
LDO
VCC
Thermal
Sensor
OTP
VCC_UVLO
VCC_UV
LO
VCS1
146.5mV
FB_OV
P
FB_OVP
OC_CO
MP
VCS1
Control Logic
Gate
Driver
8
DR
PWM_COMP
FB_OVP
7
PGND
Islope=40uA
VCS1
1
ISNS
3
COMP
5
AGND

Figure 13

Overview

The SCT81621 device is a wide input range, non-synchronous boost controller that uses peak-current-mode control. The device can be used in boost, SEPIC, and flyback topologies.

In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the ISNS pin. This voltage is fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed

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The compensation ramp has been added internally in the SCT81621. The slope of this compensation ramp has been selected to satisfy most applications, and its value depends on the switching frequency. This slope can be calculated using the formula:

$$M_c = V_{SL} * F_s \quad (9)$$

V_{SL} is the amplitude of the internal compensation ramp and F_S is the controller's switching frequency.

For more flexibility, slope compensation can be increased by adding one external resistor, R_{SL}, in the ISEN's path. Figure15 shows the setup. The externally generated slope compensation is then added to the internal slope compensation of the SCT81621. When using external slope compensation, the formula for Mc becomes:

$$M_c = (V_{SL} + K * R_{SL}) * F_s \quad (10)$$

A typical value for factor K is 40 µA.

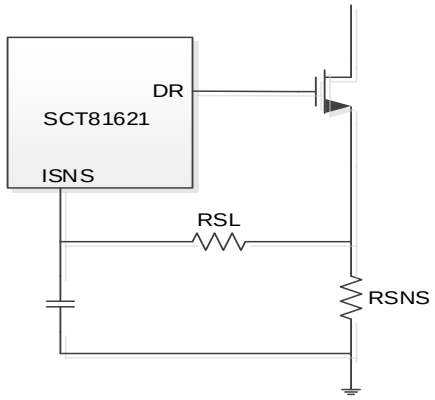


Figure15. External RSL to increase slope compensation

Adjustable Peak Current Limit

The device provides cycle-by-cycle peak current limit protection that turns off the MOSFET when the sum of the inductor current and the programmable slope compensation ramp reaches the current limit threshold. Peak inductor current limit ($I_{PEAK-CL}$) in steady state is calculated as shown in:

$$I_{PEAK_CL} = \frac{V_{SENSE} - 40uA \times R_{SL} \times D}{R_{SNS}} \quad (11)$$

Where

V_{SENSE} is ISEN pin limiting voltage (Typ. =146.5mV)
$I_{PEAK-CL}$ is the inductor peak current limit
R_{SL} is Slope compensation resistor
D is Duty cycle
R_{SNS} is the Inductance peak current detection resistance

When overload happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high. When COMP voltage is clamped for 64 cycles, the controller stops working. After remaining OFF for 32768 cycles the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high after soft start time and COMP still keep high for 64 cycles the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to

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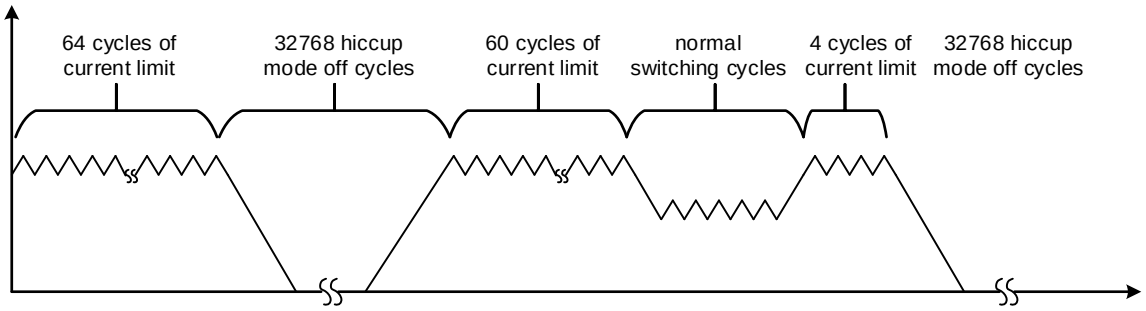


Figure16. Hiccup Mode Protection

Because D can be variable under different Vin, $I_{PEAK-CL}$ is not stable under different Vin when using external slope compensation resistor. So for an accurate peak current limit operation over the input supply voltage, SCT recommends using only the fixed slope compensation.

Output Voltage

The output voltage is set by an external resistor divider RFBT and RFBB in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of RFBT can be calculated by Equation 12.

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (12)$$

where:

V_{REF} is the feedback reference voltage, typical 1.275V

Frequency Adjust/Shutdown/ Synchronization

The switching frequency of the SCT81621 can be adjusted between 100 kHz and 2.2 MHz using a single external resistor. This resistor must be connected between the FA/SYNC/SD pin and ground. Equation 13 can be used to estimate the frequency adjust resistor.

$$R_{FA}(K\Omega) = \frac{19700}{fsw(kHz)} - 1.177 \quad (13)$$

The SCT81621 can also be synchronized to an external clock. The external clock must be connected between the FA/SYNC/SD pin and ground, as shown in Figure 17. The frequency adjust resistor may remain connected while synchronizing a signal, therefore if there is a loss of signal, the switching frequency will be set by the frequency adjust resistor.

The FA/SYNC/SD pin also functions as a shutdown pin. If a high signal (>1.27V) appears on the FA/SYNC/SD pin over 30 S, the SCT81621 stops switching and goes into a low current mode. The total supply current of the IC reduces to 3.9 µA, typically, under these conditions.

Figure 19 and Figure 20 show an implementation of a shutdown function when operating in frequency adjust mode and synchronization mode, respectively. In frequency adjust mode, connecting the FA/SYNC/SD pin to ground forces the clock to run at a certain frequency. Pulling this pin high shuts down the IC. In frequency adjust or

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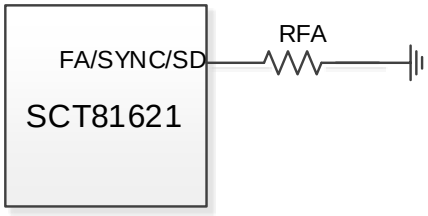


Figure17. Frequency Adjust

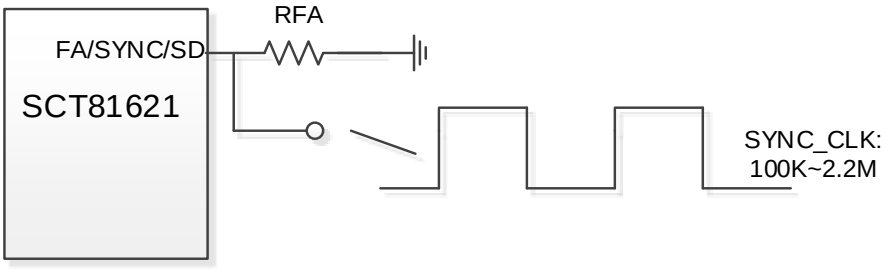


Figure18. Frequency Sync

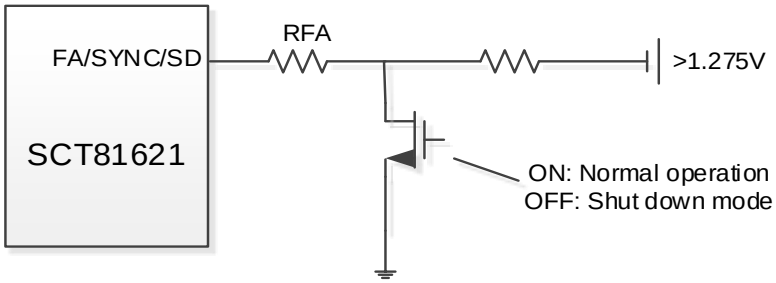


Figure19. Shutdown operation in Frequency Adjust Mode

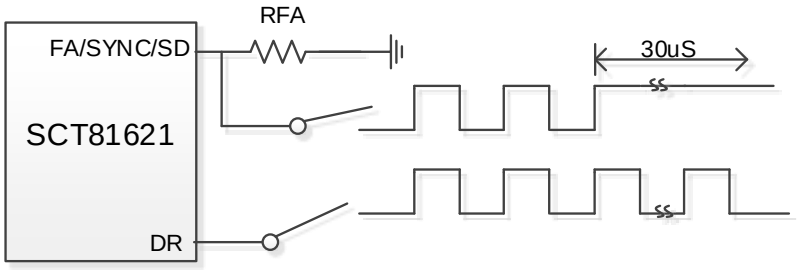


Figure20. Shutdown operation in Frequency Synchronization Mode

Enable and Under Voltage Lockout Threshold

The external UVLO resistor divider must be designed so that the voltage at the UVLO pin is greater than 1.42 V typical) when the input voltage is in the desired operating range. The values of R1 and R2 can be calculated as shown in Equation 14 and Equation 15.

$$R1 = \frac{V_{IN(ON)} - V_{IN(OFF)}}{I_{UVLO}} \quad (14)$$

where

$V_{IN(ON)}$ is the desired start-up voltage of the converter
$V_{IN(OFF)}$ is the desired turnoff voltage of the converter.

$$R2 = R1 * \frac{V_{UVLOEN}}{V_{IN(ON)} - V_{UVLOEN}} \quad (15)$$

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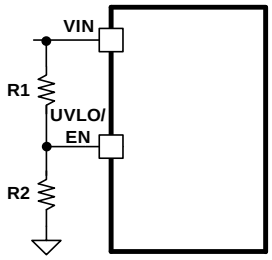


Figure21. System UVLO Resistor Divider

Frequency Spread Spectrum

To reduce EMI, the device implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching

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The total power dissipation of the IC (PD) can be calculated by the following formula: PD = (VIN × IIN) - (VOUT × IOUT) = VIN × IIN - VOUT × IOUT

Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

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The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

Output Diode Selection

The diode at the output side must withstand the reverse voltage when the MOSFET is turned-on. The peak reverse voltage is given by:

$$V_{D_PEAK} = V_{IN_MAX} + V_{O_MAX} \quad (37)$$

The diode should also be capable to flow switch peak current I_{Q_PEAK}.

The power dissipation of the diode is equal to the forward voltage drop multiplies output current. Schottky diodes are recommended here to minimize the power loss.

Coupling Capacitor Selection

For ceramic capacitors with low-ESR, the peak to peak voltage ripple on coupling capacitor is estimated by:

$$\Delta V_{CS} = \frac{I_O \times D_{MAX}}{C_S \times f_{SW}} \quad (38)$$

The maximum voltage across the coupling capacitor is maximum input voltage. The voltage rating of the coupling capacitor must be greater than it.

The RMS current of coupling capacitor is given by:

$$I_{CS_RMS} = I_O \times \sqrt{\frac{V_O + V_D}{V_{IN_MIN}}} \quad (39)$$

There is a large RMS current through coupling capacitor relative to output power. Ensure the coupling capacitor can withstand it with good heat generation to have proper thermal performance.

Input Capacitor Selection

The SEPIC has an inductor at input side thus the input current is continuous and triangular. BT/C*392 792gumal performance.

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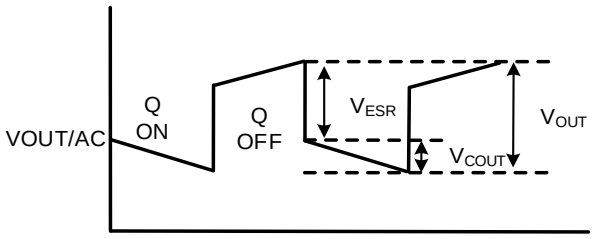


Figure 30. Output Voltage Ripple

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Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted



Figure 31. Power up(Iload=2A)

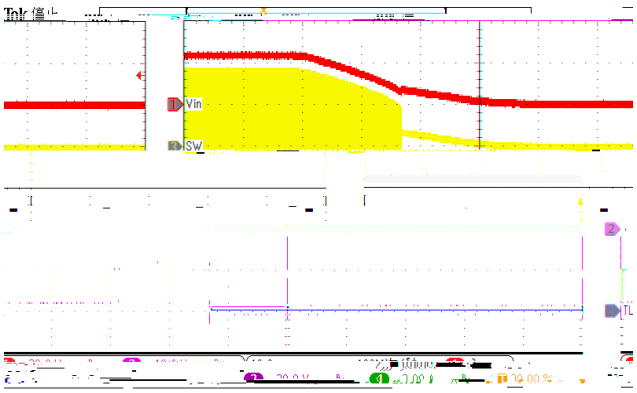


Figure 32. Power down(Iload=2A)



Figure 33. Shutdown entry

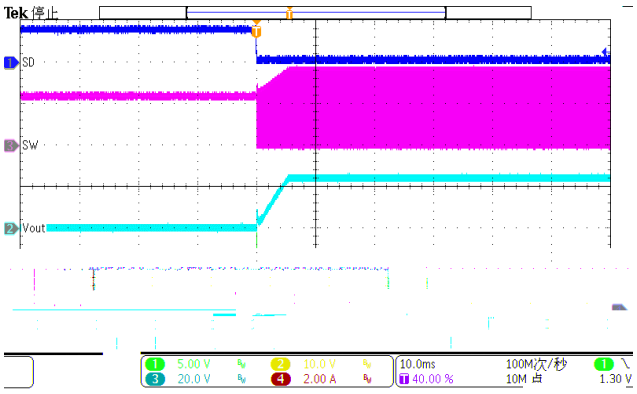


Figure 34. Shutdown remove

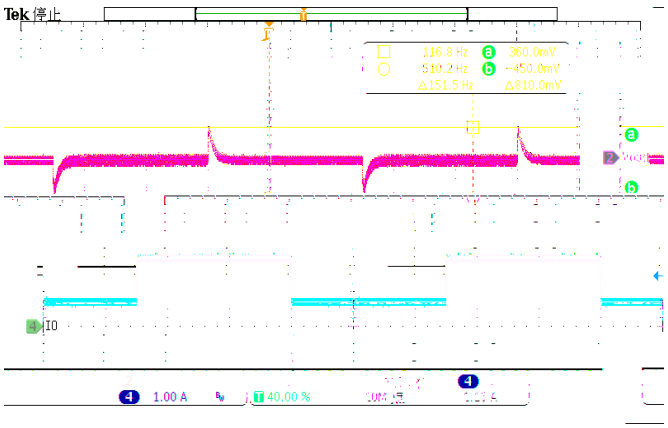


Figure 35. LoadTrans (Iload=0.5A-1.5A)

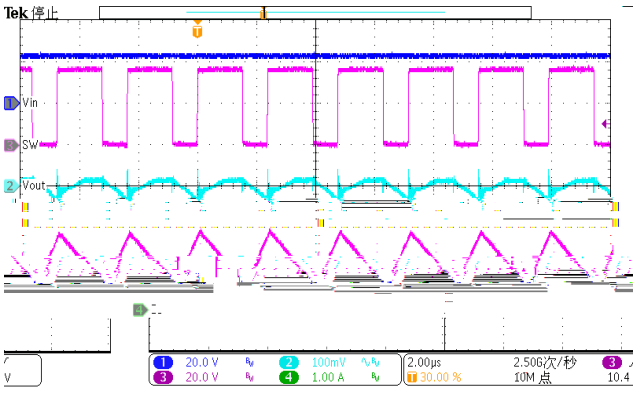
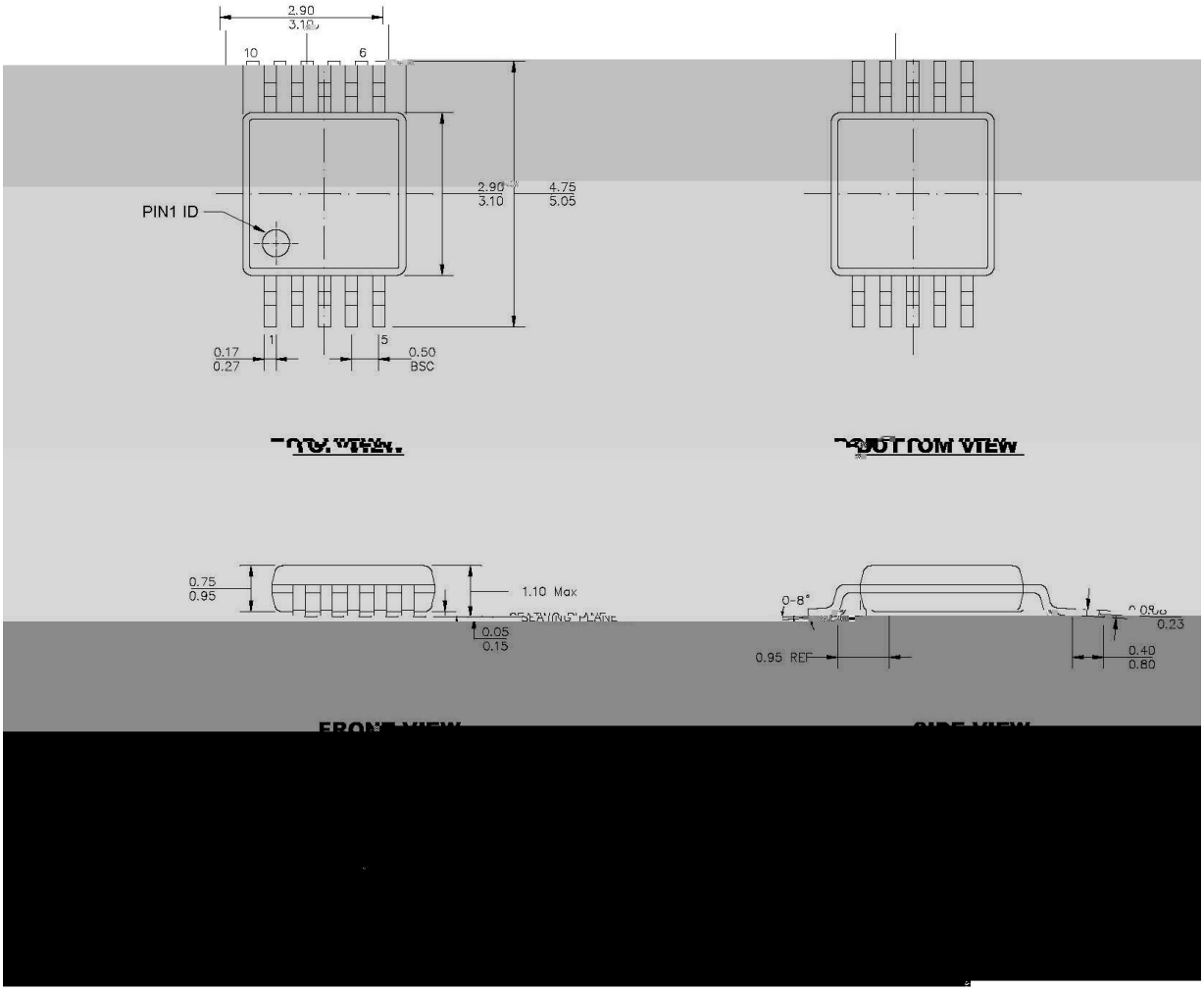
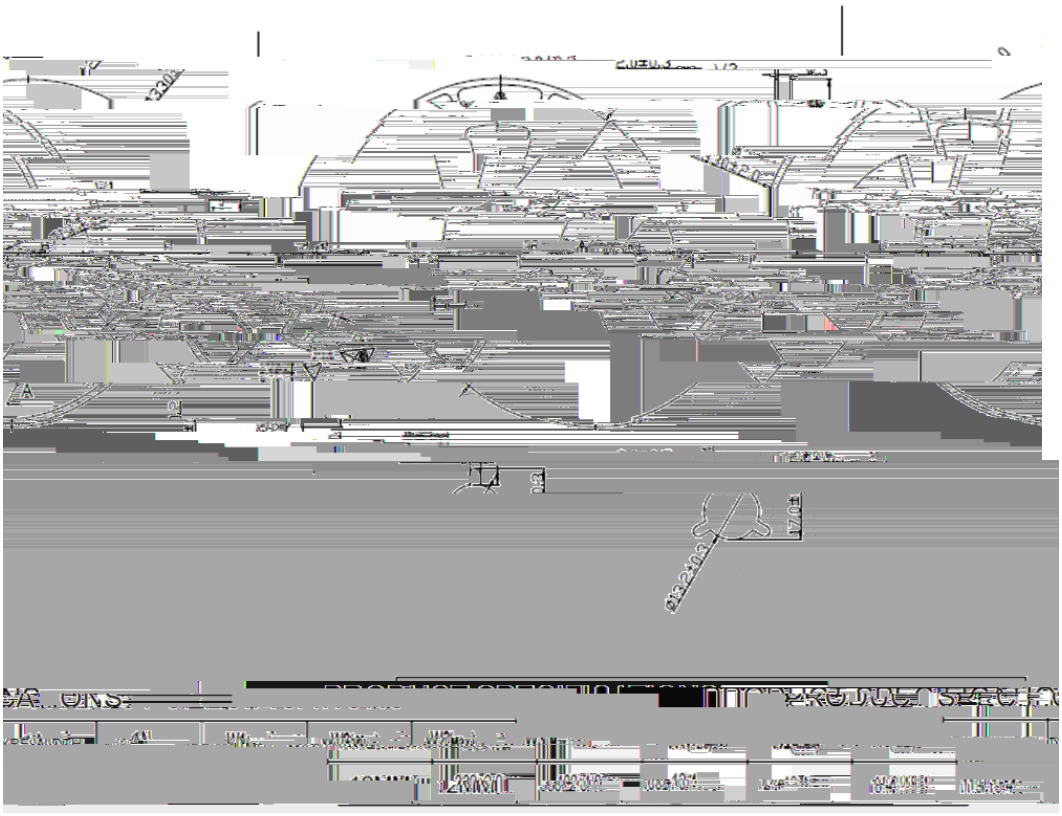
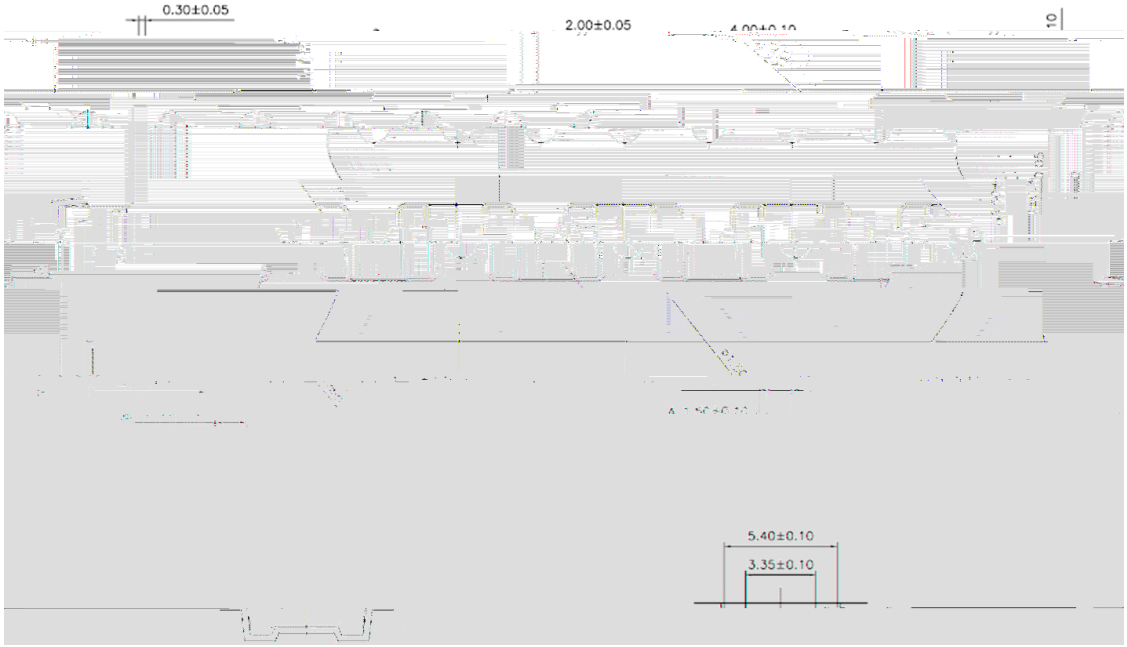


Figure 36. steady-state (Iload=2A)

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2.90
3.10
10
6
PIN1 ID
2.90
3.10
4.75
5.05
0.17
0.27
1
5
0.50
BSC
0.75
0.95
1.10 Max
0.05
0.15
0-8°
0.95 REF
0.23
0.40
0.80





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